

Rockchip RK805 Datasheet

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Revision History

| Date | Revision | Description |
|-------------|-----------------|--------------------------|
| 2018-12-24 | 1.3 | Order information update |
| 2017-3-29 | 1.2 | Power sequence change |
| 2016-9-21 | 1.1 | Update |
| 2016-9-9 | 1.0 | Initial release |

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Chapter 1 Introduction

1.1 Overview

The RK805 is a complete power supply solution for Portable systems. The highly integrated device includes four buck DC-DC converters, three high performance Ldos, I²C interface, programmable power sequencing and an RTC.

The RK805 improves performance, reduces component count and size, and therefore provides lower cost solution compared to conventional portable designs. The ultra fast 2MHz current mode DC/DC architecture optimizes the transient performance and is compatible with tiny low cost ceramic inductors and capacitors. All DC/DC channels include integrated MOSFETS. Internal soft-start and compensation circuits minimize external components count. Most outputs can be programmed through the I²C interface

The RK805 integrates internal RC oscillator for low cost application which without RTC function.

1.2 Feature

- Input voltage range: 2.7V to 5.5V
- 2MHz Switching Frequency for bucks
- Current mode architecture for best transient performance
- Internal compensation and soft start
- I²C Programmable output levels and power sequencing
- High efficiency architecture
- Integrated Vout Discharge Circuit for BUCK and LDO
- Power:
 - CH1: Synchronous Buck regulator, 2.5A max
 - CH2: Synchronous Buck regulator, 2.5A max
 - CH3: Synchronous Buck regulator, 1.5A max
 - CH4: Synchronous Buck regulator, 1.5A max
 - CH5,CH6: Linear regulators, 300mA max
 - CH7: Low noise and high PSRR linear regulator,100mA max
- Auxiliary: Flexible Power Sequence control
- Package: 4mmx4mm QFN32 (pitch 0.4mm)

1.3 Typical Application Diagrams

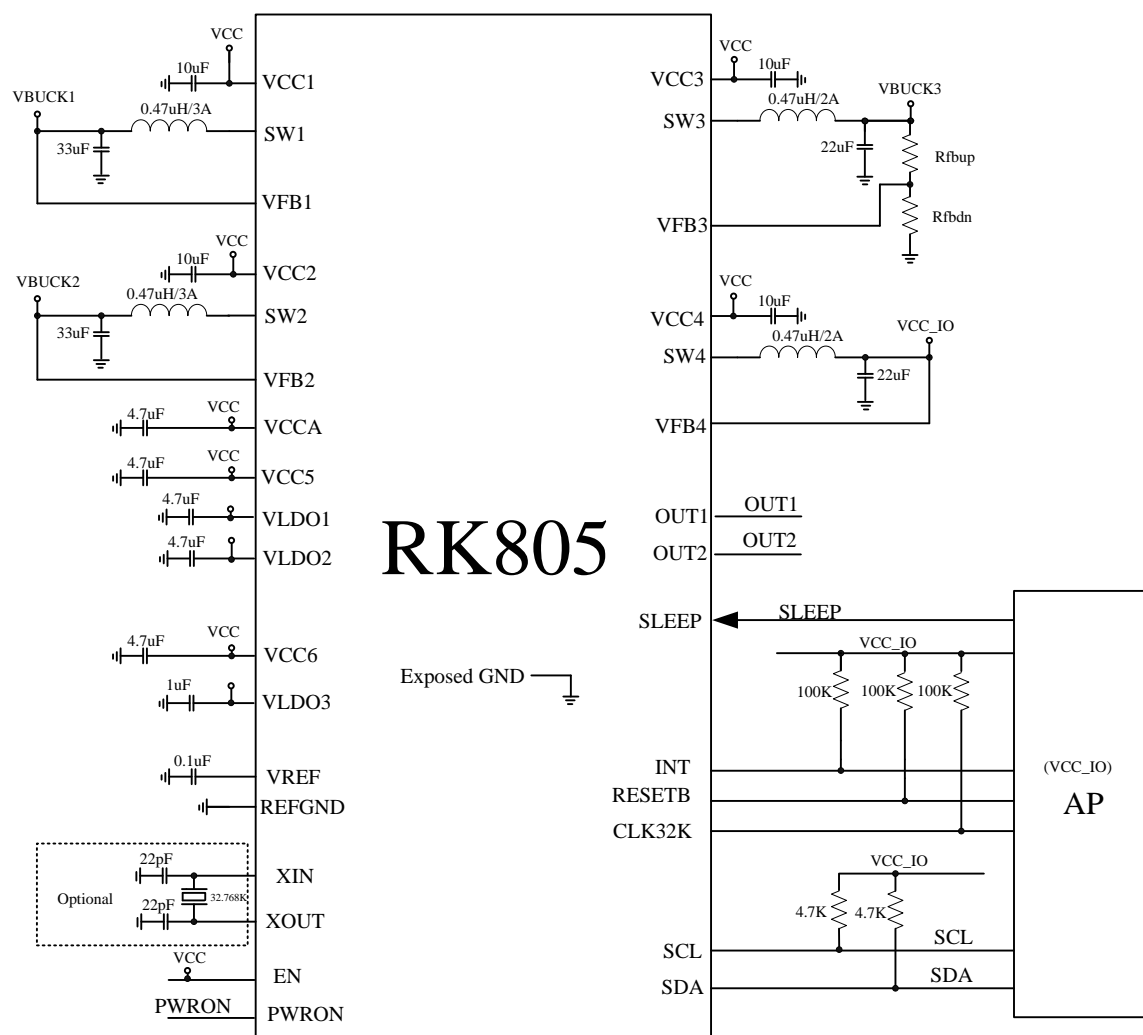


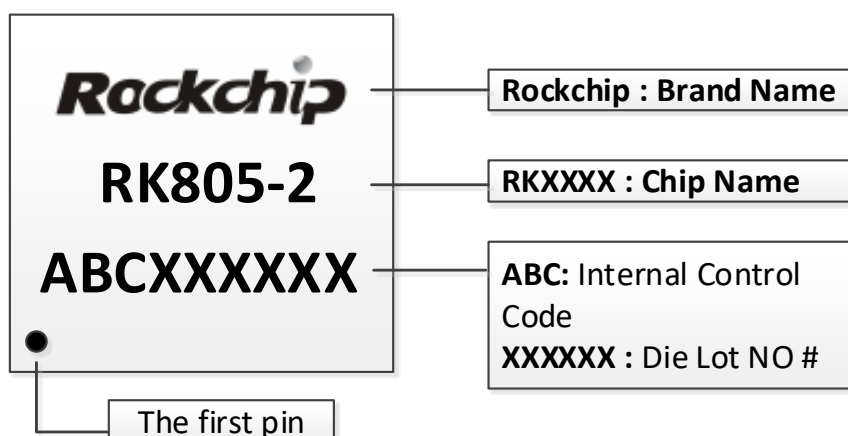
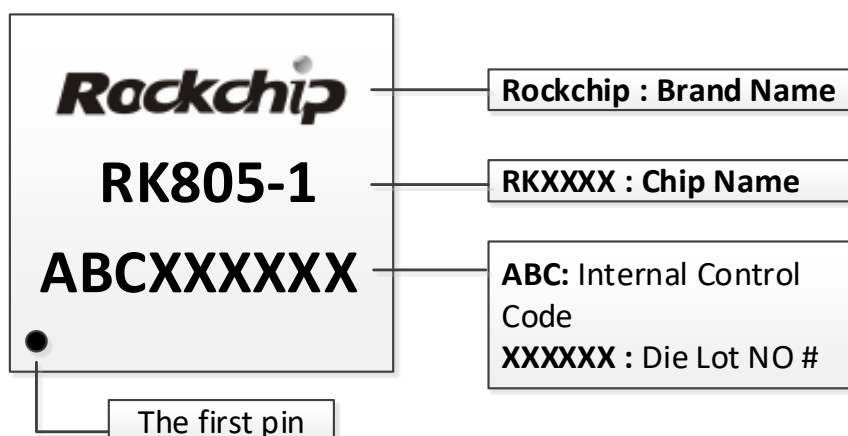
Fig. 1-1 RK805 One Battery Cell Application

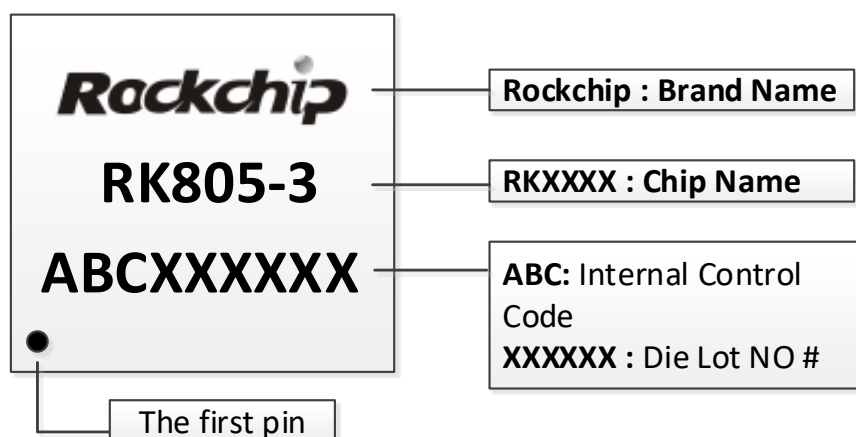
Chapter 2 Package information

2.1 Ordering information

| Orderable Device | RoHS status | Package | Package Qty | Device special feature |
|------------------|-------------|------------|-----------------------------|------------------------|
| RK805-1 | RoHS pass | QFN32(4X4) | 2000ea by reel/inner box* 5 | For RK3228 application |
| RK805-2 | RoHS pass | QFN32(4X4) | 2000ea by reel/inner box* 5 | For RK1108 application |
| RK805-3 | RoHS pass | QFN32(4X4) | 2000ea by reel/inner box* 5 | For RK3128 application |

2.2 Top Marking





2.3 Dimension

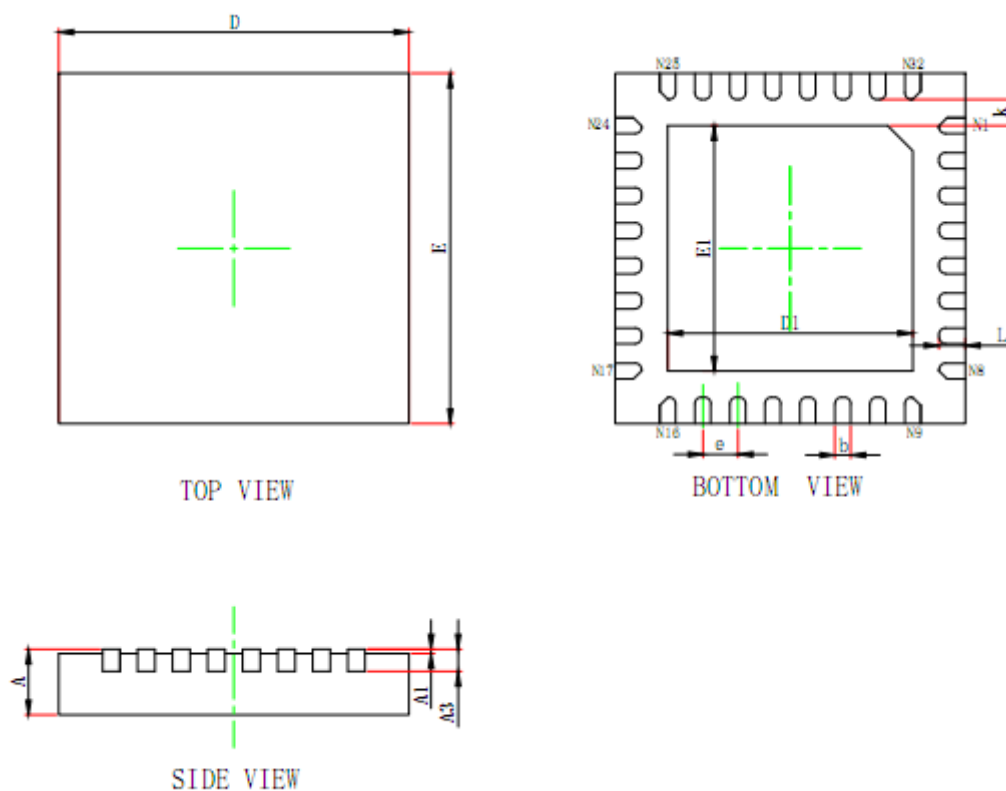


Fig. 2-1 QFN32 4mm X 4mm (Pitch is 0.4mm)

| DESCRIPTION | SYMBOL | MILLIMETER | | |
|--------------------|--------|----------------------|----------------------|-----------|
| | | MIN | NOM | MAX |
| TOTAL THICKNESS | A | 0.70/0.80 | | 0.80/0.90 |
| STAND OFF | A1 | 0 | 0.035 | 0.05 |
| MATERIAL THICKNESS | A3 | - | 0.203 _{REF} | - |
| PACKAGE SIZE | D | 3.924 | | 4.076 |
| | E | 3.924 | | 4.076 |
| EP SIZE | D1 | 2.700 | | 2.900 |
| | E1 | 2.700 | | 2.900 |
| LEAD LENGTH | L | 0.224 | | 0.376 |
| LEAD PITCH | e | 0.400 _{TYP} | | |
| LEAD WIDTH | b | 0.150 | | 0.250 |
| LEAD TO EXPOSED | k | 0.200 _{MIN} | | |

Note:

- Coplanarity applies to leads, corner leads and die attach pad.
- Dimension b applies to metalized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measure in that radius area.
- 0.15mm of dimension b is recommended in PCB layout.

2.4 Pin Assignment

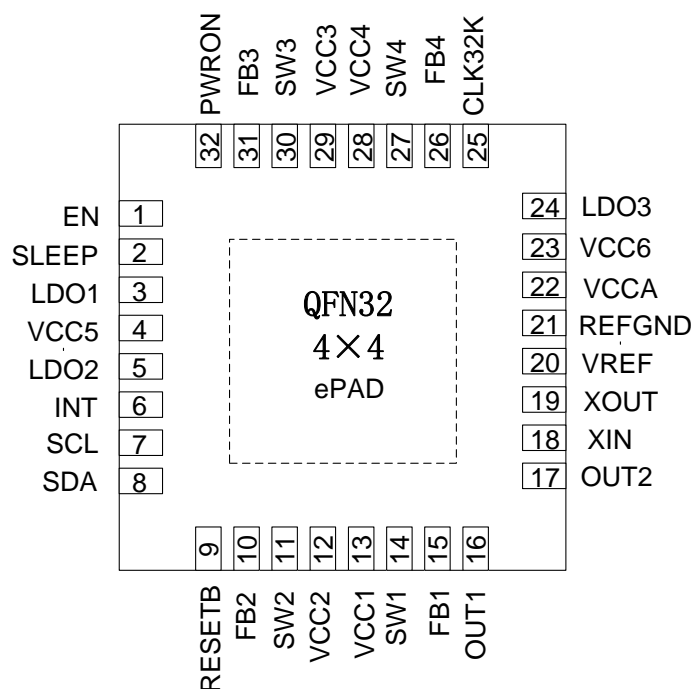


Fig. 2-2 Pin Assignment

2.5 Pinout Number Order

| PIN NO | PIN NAME | PIN DESCRIPTION |
|--------|----------|--|
| 1 | EN | Power on or power off enable pin, active high, internal 800k resistor pull low to ground |
| 2 | SLEEP | Sleep mode control input |
| 3 | LDO1 | LDO1 output |
| 4 | VCC5 | Power supply of LDO1/2 |
| 5 | LDO2 | LDO2 output |
| 6 | INT | Interrupt request pin, open drain |
| 7 | SCL | I2C clock input |
| 8 | SDA | I2C data input and output |
| 9 | RESETB | Reset pin after power on, active low |
| 10 | FB2 | Output feedback voltage of buck2 |
| 11 | SW2 | Switching node of buck2 |
| 12 | VCC2 | Power supply of buck2 |
| 13 | VCC1 | Power supply of buck1 |
| 14 | SW1 | Switching node of buck1 |
| 15 | FB1 | Output feedback voltage of buck1 |
| 16 | OUT1 | General digital output pin 1, CMOS level output, high level is VFB4 |

| PIN NO | PIN NAME | PIN DESCRIPTION |
|-------------|----------------|---|
| 17 | OUT2 | General digital output pin 2, CMOS level output, high level is VFB4 |
| 18 | XIN | 32.768KHz crystal oscillator input |
| 19 | XOUT | 32.768KHz crystal oscillator output |
| 20 | VREF | Internal reference voltage |
| 21 | REFGND | Reference ground |
| 22 | VCCA | Power supply of controller |
| 23 | VCC6 | Power supply of LDO3 |
| 24 | LDO3 | LDO3 output |
| 25 | CLK32K | 32.768KHz clock output, open drain |
| 26 | FB4 | Output feedback voltage of buck4 |
| 27 | SW4 | Switching node of buck4 |
| 28 | VCC4 | Power supply of buck4 |
| 29 | VCC3 | Power supply of buck3 |
| 30 | SW3 | Switching node of buck3 |
| 31 | FB3 | Output feedback voltage of buck3 |
| 32 | PWRON | Power on key input, active low, internal 17k resistor pull high to VCCA |
| Exposed pad | Exposed ground | Ground |

Chapter 3 Electrical Characteristics

3.1 Absolute Maximum Ratings

| Parameter | Min | Max | Units |
|---|------|--------------|-------|
| Voltage range on pins VCCx, SWx, FBx | -0.3 | 6.5 | V |
| Voltage range on pins LDOx, VREF | -0.3 | 6.5 | V |
| Voltage range on pin CLK32K, SLEEP | -0.3 | 6.5 | V |
| Voltage range on pins XIN,XOUT, EN, PWRON | -0.3 | VCCx_MAX+0.3 | |
| Voltage range on pins RESETB, INT, SDA, SCL,OUT1,OUT2 | -0.3 | 4 | V |
| Storage temperature range, TS | -40 | 150 | °C |
| Operating temperature range, TJ | -40 | 125 | °C |
| Maximum Soldering Temperature, T _{SOLDER} | | 300 | °C |

Note 1. Exposure to the conditions exceeded absolute maximum ratings may cause the permanent damages and affect the reliability and safety of both device and systems using the device. The functional operations cannot be guaranteed beyond specified values in the recommended conditions.

3.2 Recommended Operating Conditions

| Parameter | Min | TYP | Max | Units |
|-----------------------------|-----|-----|-----|-------|
| Voltage range on pins VCCx | 2.7 | 5 | 5.5 | V |
| Voltage range on other pins | | | 5.5 | V |
| Power Dissipation | | | 2.7 | W |

3.3 DC Characteristics

T_J=25°C; V_{VCCA}=VCCx=5V, unless otherwise specified.

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|--|----------------------|---|--------|------|-------|-------|
| VCCA Input (VCCA is the power supply of controller) | | | | | | |
| VCCA Operating Range | V _{VCCA} | | 2.8 | 5 | 5.5 | V |
| VCCA over voltage protect | V _{VCCA_ov} | | | 6 | | V |
| VCCA under voltage protect | V _{VCCA_uv} | Step=0.1V, from 2.7V to 3.4V programmable | | 2.7 | | V |
| VCCA low voltage alarm | V _{VCCA_lv} | Step=0.1V, from 2.8V to 3.5V programmable | | 3.3 | | V |
| VCCA OK voltage threshold | V _{VCCA_ok} | 2.8V/3.0V/3.4V/3.6V OTP programmable | | 3.0 | | V |
| CH1: Buck 1 | | | | | | |
| Input supply voltage range | V _{CC1} | | 2.7 | | 5.5 | V |
| Voltage Adjustable Range, 6bit | V _{FB1} | 0.7125V~1.45V (Step=12.5mV)/1.8V/2.0V/2.2V/2.3V | 0.7125 | | 2.300 | V |
| Rated output current | I _{MAX1} | | | 2.5 | | A |
| Output voltage transition rate | dV/dt | BUCK1_RATE=00 | | 3 | | mV/uS |
| | | BUCK1_RATE=01 | | 6 | | |
| | | BUCK1_RATE=10 | | 12.5 | | |
| | | BUCK1_RATE=11 | | 25 | | |

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|------------------------|--|--------|-------|-------|-------|
| CH1: Buck 2 | | | | | | |
| Input supply voltage range | V _{CC2} | | 2.7 | | 5.5 | V |
| Voltage Adjustable Range, 6bit | V _{FB2} | 0.7125V~1.45V (Step=12.5mV)/1.8V/2.0V/2.2V/2.3V | 0.7125 | | 2.300 | V |
| Rated output current | I _{MAX2} | | | 2.5 | | A |
| Output voltage transition rate | dV/dt | BUCK1_RATE=00 | | 3 | | mV/uS |
| | | BUCK1_RATE=01 | | 6 | | |
| | | BUCK1_RATE=10 | | 12.5 | | |
| | | BUCK1_RATE=11 | | 25 | | |
| CH1: Buck 3 | | | | | | |
| Input supply voltage range | V _{CC3} | | 2.7 | | 5.5 | V |
| Feedback Voltage | V _{FB3} | | 0.784 | 0.800 | 0.816 | V |
| Rated output current | I _{MAX3} | | | 1.5 | | A |
| V _{BUCK3OUT} = V _{FB3} * (1+R _f bup/R _f bdn); please refer to the typical application | | | | | | |
| CH1: Buck 4 | | | | | | |
| Input supply voltage range | V _{CC4} | | 2.7 | | 5.5 | V |
| Voltage Adjustable Range, 5bit | V _{FB4} | Step=100mV | 0.8 | | 3.5 | V |
| Rated output current | I _{MAX4} | | | 1.5 | | A |
| CH5 : LDO1 | | | | | | |
| Input supply voltage range | V _{CC5} | | 2.0 | | 5.5 | V |
| V _{OUT} Output Voltage Adjustable Range, 5bit | V _{LDO1} | Step=100mV | 0.8 | | 3.4 | V |
| Rated output current | I _{MAX5} | V _{CC5} =5V | | 300 | | mA |
| Power supply reject ratio (f=1kHz) | PSRR1 | V _{CC5} =5V,V _{LDO1} =1V | | 50 | | dB |
| Drop-out voltage @ 300mA | V _{drop-out1} | V _{LDO1} =3.4V, | | 200 | | mV |
| CH6 : LDO2 | | | | | | |
| Input supply voltage range | V _{CC5} | | 2.0 | | 5.5 | V |
| V _{OUT} Output Voltage Adjustable Range, 5bit | V _{LDO2} | Step=100mV | 0.8 | | 3.4 | V |
| Rated output current | I _{MAX6} | V _{CC5} =5V | | 300 | | mA |
| Power supply reject ratio (f=1kHz) | PSRR2 | V _{CC5} =5V,V _{LDO2} =1.8V | | 50 | | dB |
| Drop-out voltage @ 300mA | V _{drop-out2} | V _{LDO2} =3.4V, | | 200 | | mV |
| CH7 : LDO3 | | | | | | |
| Input supply voltage range | V _{CC6} | | 2.0 | | 5.5 | V |
| V _{OUT} Output Voltage Adjustable Range, 5bit | V _{LDO3} | Step=100mV | 0.8 | | 3.4 | V |
| Rated output current | I _{MAX7} | V _{CCA} =5V | | 100 | | mA |
| Power supply reject ratio (f=1kHz) | PSRR3 | V _{CCA} =5V,V _{LDO3} =1.0V | | 70 | | dB |
| Drop-out voltage @ 100mA | V _{drop-out3} | V _{LDO3} =3.4V, | | 200 | | mV |
| I2C Interface(7 bits I2C slave address:0011000) | | | | | | |
| SCL clock frequency | f _{SCL} | | | | 1 | MHz |
| RTC | | | | | | |
| RTC operation voltage | | | 2.5 | | 5.5 | V |
| CLK32K Jitter | | | | 100 | | nS |
| CLK32K duty | | | 40 | | 60 | % |

Chapter 4 Function Description

4.1 State Machine Description

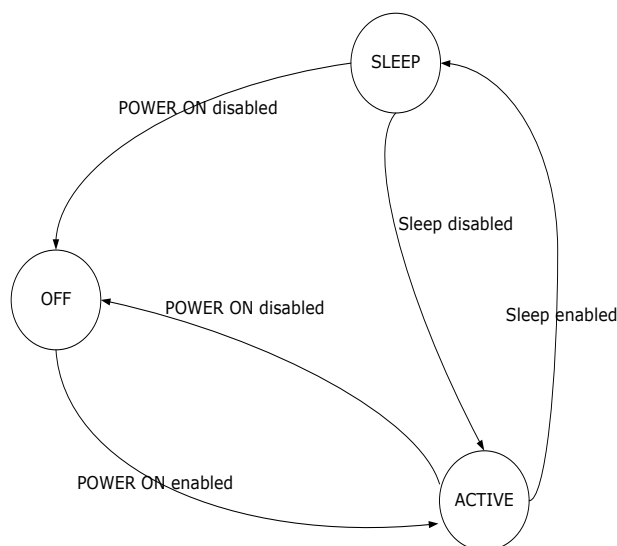


Fig. 4-1 State Machine

4.2 Device Power on Enable Conditions

- If none of the device power-on disable conditions is met, the following conditions are available to turn on the device:
 - EN signal rise edge.
 - EN signal is high level, and PWRON signal keep low level at lease 500mS while the device is off.
 - EN signal is high level, and RTC alarm interrupt flag active while the device is off.

4.3 Device Power on Disable Conditions

- EN signal keep low level.
- PWRON signal low level during more than the long-press delay: TDPWRONLP.
- Die temperature has reached the thermal shutdown threshold.
- VCCA down below UVLO threshold.
- VCCA down below VBLO threshold, and Reg21<4>=0.
- VCCA higher than OVP threshold.
- SLEPP signal active, and Reg50<3:2>=1X
- DEV_OFF control bit set to 1.

4.4 Device Sleep Enable Conditions

- SLEEP signal high level and Reg50<1>=1, and Reg50<3:2>=01.
- SLEEP signal low level and Reg50<1>=0, and Reg50<3:2>=01.
- Reg4b<1>=1.

4.5 Power Sequence

| AP | | | Null | | RK3228 | | RK1108 | | RK3128 | |
|-----------|--|--------------------|---------|-----|---------|-----|---------|-----|---------|-----|
| BOOT(OTP) | | | 0 | | 1 | | | | | |
| | | | RK805-0 | | RK805-1 | | RK805-2 | | RK805-3 | |
| | Output voltage range | Max output current | Volt | SEQ | Volt | SEQ | Volt | SEQ | Volt | SEQ |
| | | | | | | | | | | |
| BUCK1 | 0.7125V-1.45V (step 12.5mV) /1.8V/2V/2.2V/2.3V | 2.5A | 1.0V | 2 | 1.1V | 2 | 1.0V | 3 | 1.1V | 2 |
| BUCK2 | 0.7125V-1.45V (step 12.5mV) /1.8V/2V/2.2V/2.3V | 2.5A | 1.0V | 2 | 1.1V | 2 | 2.2V | 1 | 1.1V | 1 |
| BUCK3 | setting by external resistors | 1.5A | X | 3 | X | 3 | X | 4 | X | 3 |
| BUCK4 | 0.8V-3.5V (step=0.1V) | 1.5A | 3.3V | 5 | 3.3V | 5 | 3.3V | 6 | 3.3V | 1 |
| LDO1 | 0.8V-3.4V (step=0.1V) | 300mA | 1.0V | 1 | 1.8V | 4 | 1.0V | 2 | 3.3V | 4 |
| LDO2 | 0.8V-3.4V (step=0.1V) | 300mA | 1.8V | 4 | 1.8V | 4 | 1.8V | 5 | 0 | X |
| LDO3 | 0.8V-3.4V (step=0.1V) | 100mA | 1.0V | 1 | 1.0V | 1 | 1.0V | 2 | 1.1V | 1 |
| RESET B | | | X | 8 | X | 10 | X | 10 | X | 10 |

Table 4-1 Power Start Up Sequence

X: The buck3 voltage is decided by external resistors. The RESETB is open drain output.

4.5.1 BOOT = 0 (RK805-0)

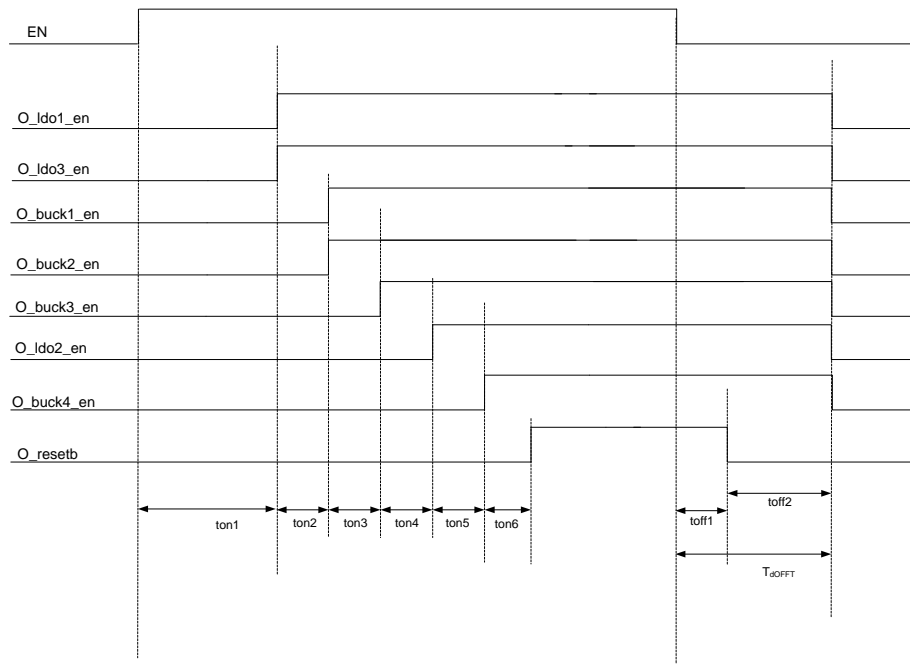
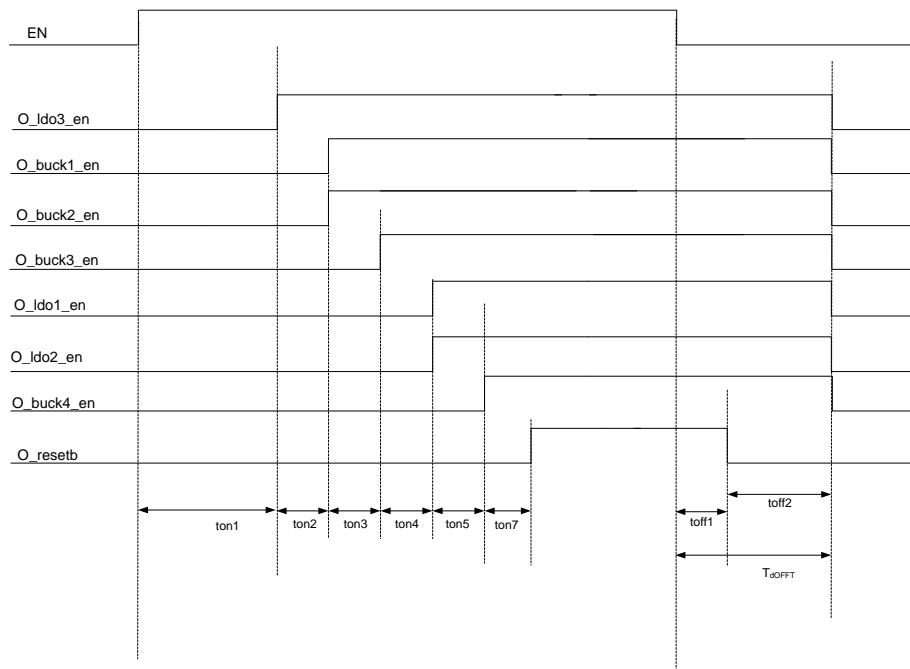


Fig. 4-2 Power On/Off Timing, B00T=0 (RK805-0)

4.5.2 BOOT = 1 (RK805-1)



4.6 Boot Timing Characteristic

| PARAMETERS | DESCRIPTION | MIN | TYP | MAX | UNIT |
|------------|--|-----|----------------------|-----|------|
| Ton1 | Reference and system ready 1st channel enable delay | | 6 | | ms |
| Ton2 | 1st channel enable delay to 2nd channel enable delay | | 2 | | ms |
| Ton3 | 2nd channel enable to 3rd channel enable delay | | 2 | | ms |
| Ton4 | 3rd channel enable to 4th channel enable delay | | 2 | | ms |
| Ton5 | 4th channel enable to 5th channel enable delay | | 2 | | ms |
| Ton6 | 5th channel enable to RESET enable delay @ RK805-0 | | 6 | | ms |
| Ton7 | 5th channel enable to RESET enable delay @ RK805-1/2 | | 10 | | ms |
| toff1 | power disable to RESETB falling delay | | $1 \times t_{CK32K}$ | | us |
| Toff2 | RESETB falling delay to supplies disable delay | | 2 | | ms |
| Ton1 | Reference and system ready 1st channel enable delay | | 6 | | ms |
| Ton2 | 1st channel enable delay to 2nd channel enable delay | | 2 | | ms |

Table 4-2 Boot Timing Characteristics

Chapter 5 Register Description

5.1 Register Summary

| HEX ADDRESS | ACTION/ DESCRIPTION | R/W | DEFAULT/ RESET |
|-------------------------------------|------------------------|-----|-----------------------------------|
| RTC Register | | | |
| 00 | SECONDS_REG | RW | 0x00 |
| 01 | MINUTES_REG | RW | 0x50 |
| 02 | HOURS_REG | RW | 0x08 |
| 03 | DAYS_REG | RW | 0x21 |
| 04 | MONTHS_REG | RW | 0x01 |
| 05 | YEARS_REG | RW | 0x16 |
| 06 | WEEKS_REG | RW | 0x04 |
| 08 | ALARM_SECONDS_REG | RW | 0x00 |
| 09 | ALARM_MINUTES_REG | RW | 0x00 |
| 0A | ALARM_HOURS_REG | RW | 0x00 |
| 0B | ALARM_DAYS_REG | RW | 0x01 |
| 0C | ALARM_MONTHS_REG | RW | 0x01 |
| 0D | ALARM_YEARS_REG | RW | 0x00 |
| 10 | RTC_CTRL_REG | RW | 0x00 |
| 11 | RTC_STATUS_REG | RW | 0x82 |
| 12 | RTC_INT_REG | RW | 0x00 |
| 13 | RTC_COMP_LSB_REG | RW | 0x00 |
| 14 | RTC_COMP_MSB_REG | RW | 0x00 |
| 20 | CLK32KOUT_REG | RW | 0x01 |
| Version Register | | | |
| 17 | CHIP_NAME_REG | RO | 0x80 |
| 18 | CHIP_VER_REG | RO | 0x50 |
| 19 | OTP_VER_REG | RO | 0000/otp<3:0> |
| PMU Control Register | | | |
| 21 | VB_MON_REG | RW | 0x14 |
| 22 | VB_UV_REG/THERMAL_REG | RW | 0x00 |
| 47 | PWRON_LP_INT_TIME_REG | RW | 0x20 |
| 48 | PWRON_DB_REG | RW | 0x40 |
| 4B | DEV_CTRL_REG | RW | 0x00 |
| 4C | INT_STS_REG | RW | 0x00 |
| 4D | INT_STS_MSK_REG | RW | 0x00 |
| 50 | IO_POL_REG | RW | 0x02 |
| 52 | OUT_REG | RW | 0x00 |
| AE | ON_SOURCE_REG | RO | 0x00 |
| AF | OFF_SOURCE_REG | RO | 0x00 |
| Power Chanel Enable Register | | | |
| 23 | DCDC_EN_REG | RW | Boot0:0x0F Boot1:0000/otp<3:0> |
| 25 | SLP_DCDC_EN_REG | RW | Boot0:0x0F Boot1:0000/otp<3:0> |

| HEX ADDRESS | ACTION/ DESCRIPTION | R/W | DEFAULT/ RESET |
|--|---------------------|-----|---|
| 26 | SLP_LDO_EN_REG | RW | Boot0:0x07 Boot1:00000/otp<2:0> |
| 27 | LDO_EN_REG | RW | Boot0:0x07 Boot1:00000/otp<2:0> |
| 2A | BUCK_LDO_SLP_LP_REG | RW | Boot0:0x07 Boot1:00000/otp<0>/0 0 |
| BUCK and LDO Configure Register | | | |
| 2E | BUCK1_CONFIG_REG | RW | 0x7A |
| 2F | BUCK1_ON_VSEL_REG | RW | Boot0:0x17 Boot1:00/otp<5:0> |
| 30 | BUCK1_SLP_VSEL_REG | RW | Boot0:0x17 Boot1:00/otp<5:0> |
| 32 | BUCK2_CONFIG_REG | RW | 0x7A |
| 33 | BUCK2_ON_VSEL_REG | RW | Boot0:0x17 Boot1:00/otp<5:0> |
| 34 | BUCK2_SLP_VSEL_REG | RW | Boot0:0x17 Boot1:00/otp<5:0> |
| 36 | BUCK3_CONFIG_REG | RW | 0x2A |
| 37 | BUCK4_CONFIG_REG | RW | 0x2A |
| 38 | BUCK4_ON_VSEL_REG | RW | Boot0:0x19 Boot1:000/otp<4:0> |
| 39 | BUCK4_SLP_VSEL_REG | RW | Boot0:0x19 Boot1:000/otp<4:0> |
| 3B | LDO1_ON_VSEL_REG | RW | Boot0:0x22 Boot1:001/otp<4:0> |
| 3C | LDO1_SLP_VSEL_REG | RW | Boot0:0x02 Boot1:000/otp<4:0> |
| 3D | LDO2_ON_VSEL_REG | RW | Boot0:0x2A Boot1:001/otp<4:0> |
| 3E | LDO2_SLP_VSEL_REG | RW | Boot0:0x0A Boot1:000/otp<4:0> |
| 3F | LDO3_ON_VSEL_REG | RW | Boot0:0x22 Boot1:001/otp<4:0> |
| 40 | LDO3_SLP_VSEL_REG | RW | Boot0:0x02 Boot1:000/otp<4:0> |

NOTE: Address 51h through 97h are for OTP registers. Customer's accessibility to those addresses is not allowed.

5.2 Register Description

5.2.1 RTC Registers

● SECONDS_REG : RTC SECOND Register

| | | | | | | | | |
|--------------|------|------|------|----------|------|------|------|------|
| Address: 00H | | | | Type: RW | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | SEC1 | | | SEC0 | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Description

- Bit 7 Reserved
 Bit 6-4 Set the second digit of the RTC seconds (0-5)
 Bit 3-0 Set the first digit of the RTC seconds (0-9)
 Note BCD coding from 00 - 59

● **MINUTES_REG : RTC MINUTE Register**

| | | | | | | | | |
|--------------|------|------|------|------|----------|------|------|------|
| Address: 01H | | | | | Type: RW | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | MIN1 | | | MIN0 | | | |
| Default | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |

Description

- Bit 7 Reserved
 Bit 6-4 Set the second digit of the RTC minutes
 Bit 3-0 Set the first digit of the RTC minutes
 Note BCD coding from 00 - 59

● **HOURS_REG : RTC HOUR Register**

| | | | | | | | | |
|--------------|-------|------|-------|------|----------|------|------|------|
| Address: 02H | | | | | Type: RW | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | PM/AM | RESV | HOUR1 | | HOUR0 | | | |
| Default | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

Description

- Bit 7 Set PM or AM: Only used in PM-AM mode, 1: PM. 0:AM.
 Bit 6 Reserved
 Bit 5-4 Set the second digit of the RTC hours
 Bit 3-0 Set the first digit of the RTC hours
 Note HOUR1/0 BCD coding from 0-11/23

● **DAYS_REG : RTC DAY Register**

| | | | | | | | | |
|--------------|------|------|------|------|----------|------|------|------|
| Address: 03H | | | | | Type: RW | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RESV | DAY1 | | DAY0 | | | |
| Default | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |

Description

- Bit 7-6 Reserved
 Bit 5-4 Set the second digit of the RTC days
 Bit 3-0 Set the first digit of the RTC days
 Note BCD coding from 01 - 28/29/30/31

● **MONTHS_REG : RTC MONTH Register**

| | | | | | | | | |
|--------------|------|------|------|------------|----------|------|------|------|
| Address: 04H | | | | | Type: RW | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RESV | RESV | MONTH 1 | MONTH0 | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

Description

Bit 7-5 Reserved
 Bit 4 Set the second digit of the RTC months
 Bit 3-0 Set the first digit of the RTC months
 Note BCD coding from 01 - 12

● **YEARS_REG : RTC YEAR Register**

| | | | | | | | | |
|--------------|-------|------|------|------|----------|------|------|------|
| Address: 05H | | | | | Type: RW | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | YEAR1 | | | | YEAR0 | | | |
| Default | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |

Description

Bit 7-5 Set the second digit of the RTC years
 Bit 3-0 Set the first digit of the RTC years
 Note BCD coding from 00 - 99

● **WEEKS_REG : RTC WEEK Register**

| | | | | | | | | |
|--------------|------|------|------|------|----------|------|------|------|
| Address: 06H | | | | | Type: RW | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RESV | RESV | RESV | RESV | WEEK | | |
| Default | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

Description

Bit 7-3 Reserved
 Bit 2-0 Set the RTC weeks
 Note BCD coding from 1 - 7

● **ALARM_SECONDS_REG : RTC ALARM SECOND Register**

| | | | | | | | | |
|--------------|------|------------|------|------|------------|------|------|------|
| Address: 08H | | | | | Type: RW | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | ALARM_SEC1 | | | ALARM_SEC0 | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Description

Bit 7 Reserved
 Bit 6-4 Set the second digit of the RTC alarm seconds
 Bit 3-0 Set the first digit of the RTC alarm seconds
 Note BCD coding from 00 - 59

● **ALARM_MINUTES_REG : RTC ALARM MINUTE Register**

| | | | | | | | | |
|--------------|------|------------|------|------|------------|------|------|------|
| Address: 09H | | | | | Type: RW | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | ALARM_MIN1 | | | ALARM_MIN0 | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Description

| | |
|---------|---|
| Bit 7 | Reserved |
| Bit 6-4 | Set the second digit of the RTC alarm minutes |
| Bit 3-0 | Set the first digit of the RTC alarm minutes |
| Note | BCD coding from 00 - 59 |

● ALARM_HOURS_REG : RTC ALARM HOUR Register

| | | | | | | | | |
|--------------|-------------|------|-------------|-------------|----------|------|------|------|
| Address: 0AH | | | | | Type: RW | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | ALARM_PM_AM | RESV | ALARM_HOUR1 | ALARM_HOUR0 | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Description

| | |
|---------|---|
| Bit 7 | Set PM or AM: Only used in PM-AM mode, 1: PM. 0:AM. |
| Bit 6 | Reserved |
| Bit 5-4 | Set the second digit of the RTC alarm hours |
| Bit 3-0 | Set the first digit of the RTC alarm hours |
| Note | HOUR1/0 BCD coding from 0-11/23 |

● ALARM_DAYS_REG : RTC ALARM DAY Register

| | | | | | | | | |
|--------------|------|------|------------|------------|----------|------|------|------|
| Address: 0BH | | | | | Type: RW | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RESV | ALARM_DAY1 | ALARM_DAY0 | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

Description

| | |
|---------|--|
| Bit 7-6 | Reserved |
| Bit 5-4 | Set the second digit of the RTC alarm days |
| Bit 3-0 | Set the first digit of the RTC alarm days |
| Note | BCD coding from 01 - 28/29/30/31 |

● ALARM_MONTHS_REG : RTC ALARM MONTH Register

| | | | | | | | | |
|--------------|------|------|------|--------------|--------------|------|------|------|
| Address: 0CH | | | | | Type: RW | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RESV | RESV | ALARM_MONTH1 | ALARM_MONTH0 | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

Description

| | |
|---------|--|
| Bit 7-5 | Reserved |
| Bit 4 | Set the second digit of the RTC alarm months |
| Bit 3-0 | Set the first digit of the RTC alarm months |
| Note | BCD coding from 01 - 12 |

● ALARM_YEARS_REG : RTC ALARM YEAR Register

| | | | | | | | | |
|--------------|-------------|------|------|------|-------------|------|------|------|
| Address: 0DH | | | | | Type: RW | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | ALARM_YEAR1 | | | | ALARM_YEAR0 | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Description

Bit 7-4 Set the second digit of the RTC alarm years

Bit 3-0 Set the first digit of the RTC alarm years

Note BCD coding from 00 - 99

● RTC_CTRL_REG : RTC Control Register

| | | | | | | | | |
|--------------|-----------------|--------------|--------------------|---------------|---------------|---------------|-------------------------|--------------|
| Address: 10H | | | | | Type: RW | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RTC_READ SEL | GET_TI ME | SET_32_ COUNTER | TEST_M ODE | AMPM_ MODE | AUTO_ COMP | ROUND_30S (Auto Clr) | STOP_ RTC |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Description

Bit 7 RTC_READSEL: 0: Read access directly to dynamic registers.

1: Read access to static shadowed registers

Bit 6 GET_TIME: Rising transition of this register transfers dynamic registers into static shadowed registers.

Bit 5 SET_32_COUNTER: 1: set the 32-kHz counter with COMP_REG value. It must only be used when the RTC is frozen.

Bit 4 TEST_MODE: 1: test mode (Auto compensation is enable when the 32kHz counter reaches at its end)

Bit 3 AMPM_MODE: 0: 24 hours mode.
1: 12 hours mode (PM-AM mode)

Bit 2 AUTO_COMP: 0: No auto compensation RW0.
1: Auto compensation enabled

Bit 1 ROUND_30S: 1: When 1 is written, the time is rounded to the closest minute in next second. self cleared after rounding

Bit 0 STOP_RTC: 1: RTC is frozen.
0: RTC is running.
RTC_time can only be changed during RTC frozen

● RTC_STATUS_REG : RTC Status Register

| | | | | | | | | |
|--------------|------------------------------|---------------------------|------------------------------|------------------------------|------------------------------|------------------------------|-------------|------|
| Address: 11H | | | | | Type: RW | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | POWER_UP (Write 1 Clr) | ALARM (Write 1 Clr) | EVENT_1D (Write 1 Clr) | EVENT_1H (Write 1 Clr) | EVENT_1M (Write 1 Clr) | EVENT_1S (Write 1 Clr) | RUN (RO) | RESV |
| Default | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

Description

- Bit 7 POWER_UP: POWER_UP is set by a reset, is cleared by writing one in this bit.
- Bit 6 ALARM: Indicates that an alarm interrupt has been generated (bit clear by writing 1) The alarm interrupt keeps its low level, until the micro-controller writes 1 in the ALARM bit of the RTC_STATUS register. The timer interrupt is a low-level pulse (15 μ s duration).
- Bit 5 EVENT_1D: One day has occurred
- Bit 4 EVENT_1H: One hour has occurred
- Bit 3 EVENT_1M: One minute has occurred
- Bit 2 EVENT_1S :One second has occurred
- Bit 1 RUN: 0, RTC is frozen. 1, RTC is running. This bit shows the real state of the RTC
- Bit 0 RESEVERED

● RTC_INT_REG : RTC Interrupt Register

| | | | | | | | | |
|--------------|------|------|------|-------------------|--------------|--------------|-------|------|
| Address: 12H | | | | Type: RW | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | RESV | RESV | INT_SLEEP_MASK_EN | INT_ALARM_EN | INT_TIMER_EN | EVERY | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Description

- Bit 7-5 RESEVERED
- Bit 4 INT_SLEEP_MASK_EN:
1: Mask periodic interrupt while the device is in SLEEP mode
0: Normal mode, no interrupt masked.
- Bit 3 INT_ALARM_EN: Enable one interrupt when the alarm value is reached
1: Enable
0: Disable
- Bit 2 INT_TIMER_EN: Enable periodic interrupt
1: Enable
0: Disable
- Bit 1-0 EVERY: 00: every second 01: every minute 10: every hour 11: every day

● RTC_COMP_LSB_REG : RTC Comensation LSB Register

| | | | | | | | | |
|--------------|--------------|------|------|----------|------|------|------|------|
| Address: 13H | | | | Type: RW | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RTC_COMP_LSB | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Description

- Bit7-0 This register contains the number of 32-kHz periods to be added into the 32KHz counter every hour [LSB]

● RTC_COMP_MSB_REG : RTC Compensation MSB Register

| | | | | | | | | |
|--------------|--------------|------|------|----------|------|------|------|------|
| Address: 14H | | | | Type: RW | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RTC_COMP_MSB | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Description

Bit7-0 This register contains the number of 32-kHz periods to be added into the 32KHz counter every hour [MSB]

● CLK32KOUT_REG : RTC Compensation MSB Register

| | | | | | | | | |
|--------------|----------|------|------|----------|------|---------------|------|---------------|
| Address: 20H | | | | Type: RW | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESERVED | | | | | VB_UV_DB_TIME | | CLK32KOUT2_EN |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Description

Bit 7-3 Reserved

Bit 2-1 VB_UV_DB_TIME: VCCA under voltage lock out de-bounce time set:
00:2mS; 01:500uS; 10:90uS; 11:30uS

Bit 0 CLK32KOUT2_EN:
1. CLK32KOUT2 output is enabled
0. CLK32KOUT2 output is disabled

5.2.2 Version Register

● CHIP_NAME_REG : Chip Name Register

| | | | | | | | | |
|--------------|-----------------|------|------|----------|------|------|------|------|
| Address: 17H | | | | Type: RO | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | CHIP_NAME<11:4> | | | | | | | |
| Default | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Description

Bit 7-0 CHIP_NAME<11:4>: chip name high 8 bits.

● CHIP_VER_REG: Chip version Register

| | | | | | | | | |
|--------------|----------------|------|------|----------|---------------|------|------|------|
| Address: 18H | | | | Type: RO | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | CHIP_NAME<3:0> | | | | CHIP_VER<3:0> | | | |
| Default | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |

Description

Bit 7-4 CHIP_NAME<3:0>: chip name low 4 bits.

Bit 3-0 CHIP_VER<3:0>: chip version.

● OTP_VER_REG: OTP Version Register

| | | | | | | | | |
|--------------|------|------|------|----------|--------------|------|------|------|
| Address: 19H | | | | Type: RO | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | | | | OTP_VER<3:0> | | | |
| Default | 0 | 0 | 0 | 0 | OTP | | | |

Description

Bit 7-4 RESV: RESEVERED
 Bit 3-0 OTP_VER<3:0>: OTP Version NO.

5.2.3 PMU Control Register

● VB_MON_REG : Battery Voltage Monitor Register

| Address: 21H | | | | Type: RW | | | | |
|--------------|-------------------------|------|-----------------------|---------------|-----------------------|-----------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | PWRON_ST STS (RO) | RESV | VB_UV_ STS (RO) | VB_LO_ ACT | VB_LO_ STS (RO) | VB_LO_SEL | | |
| Default | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

Description

Bit 7 PWRON_ST: PWRON key status
 0: no PWRON key pressed
 1: PWRON key pressed
 This bit is read only

Bit 6 RESV: RESEVERED

Bit 5 VB_UV_STS: VCCA under voltage lockout status(shut down system if the bit=1)
 This bit is read only

Bit 4 VB_LO_ACT: VCCA low action
 0: shut down system
 1: insert interrupt

Bit 3 VB_LO_STS: VCCA low voltage status
 0: VCCA>VB_LO_SEL
 1: VCCA<VB_LO_SEL
 This bit is read only

Bit 2-0 VB_LO_SEL: VCCA low voltage threshold
 000~111: 2.8V~ 3.5V, step=100mV

● THERMAL_REG : Thermal Control Register

| Address: 22H | | | | Type: RW | | | | |
|--------------|-----------|------|------|--------------|-------------|------|------------------------|-----------------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | VB_UV_SEL | | | TSD_T EMP | HOTDIE_TEMP | | HOTDIE_ST S (RO) | TSD_STS (RO) |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Description

Bit 7-5 VB_UV_SEL: VCCA under voltage threshold
 000~111: 2.7V~ 3.4V, step=100mV

Bit 4 TSD_TEMP: Thermal shutdown temperture threshold
 0: 140°C;

1: 160°C

Bit 3-2 HOTDIE_TEMP: Hot-die temperature threshold

00: 85°C; 01: 95°C; 10: 105°C; 11: 115°C

Bit 1 HOTDIE_STS: Hot-die warning

This bit is read only bit.

Bit 0 TSD_STS: Thermal shut down

● PWRON_LP_TIME_REG: Long Press key Interrupt Time Register

| | | | | | | | | |
|--------------|------|-----------------|------|----------|------|------|------|------|
| Address: 47H | | | | Type: RW | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | PWRON_LP_TM_SEL | | RESV | | | | |
| Default | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

Description

Bit 7 RESV: RESERVED

Bit 6-5 PWRON_LP_TM_SEL: Long press PWRON key interrupt time set.
00: 0.5S, 01: 1S, 10: 1.5S, 11: 2S

Bit 4-0 RESV: RESERVED

● PWRON_DB_REG: Key De-bounce Time Register

| | | | | | | | | |
|--------------|------|--------------|------|----------|------|------|------|------|
| Address: 48H | | | | Type: RW | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | PWRON_DB_SEL | | RESV | | | | |
| Default | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

Description

Bit 7 RESV: RESERVED

Bit 6-5 PWRON_DB_SEL: PWRON key de-bounce time set.
00: 32uS, 01: 10mS, 10: 20mS, 11: 40mS

Bit 4-0 RESV: RESERVED

● DEV_CTRL_REG: Device Control Register

| | | | | | | | | |
|--------------|-----------|---------------|-------------------|----------|-------------|------|----------|---------|
| Address: 4BH | | | | Type: RW | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | INT_FC_EN | PWRO_N_LP_ACT | PWRON_LP_OFF_TIME | | DEV_OFF_RST | RESV | DEV_SL_P | DEV_OFF |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Description

Bit 7 INT_FC_EN: Interrupt watch dog enable
1: enable(Pin INT will output 2S active level, and then 10mS dis-active level)Bit 6 0: disable
Long press key action
0: Turn down PMU 1: Turn down and restart PMU

- Bit 5-4 PWRON_LP_OFF_TIME: PWRON long press time set:
00: 6S, 01: 8S, 10: 10S, 11: 12S
- Bit 3 DEV_OFF_RST: write "1" to reset PMU register.
- Bit 2 RESV: reserved
- Bit 1 DEV_SLP: write "1" to go sleep mode.
- Bit 0 DEV_OFF: write "1" to turn down the PMU.

● INT_STS_REG(REG[4C]): Interrupt Status Register

| Address: 4CH | | | | Type: RW | | | | |
|--------------|---------------------------------|---------------------------------|--------------------------------|-----------------------------|-------------------------------|----------------------------|----------------------------|---------------------------------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | PWRON_FALL_INT (Write 1 clr) | RTC_PERIOD_INT (Write 1 clr) | RTC_ALARM_INT (Write 1 clr) | HOTDIE_INT (Write 1 clr) | PWRON_LP_INT (Write 1 clr) | PWRON_INT (Write 1 clr) | VB_LO_INT (Write 1 clr) | PWRON_RISE_INT (Write 1 clr) |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Description

- Bit 7 PWRON_FALL_INT: PWRON pin falling edge interrupt status.
- Bit 6 RTC_PERIOD_INT: RTC period interrupt status.
- Bit 5 RTC_ALARM_INT: RTC alarm interrupt status.
- Bit 4 HOTDIE_INT: Hot-die interrupt status.
- Bit 3 PWRON_LP_INT: PWRON long press interrupt status.
- Bit 2 PWRON_INT: PWRON interrupt status.
- Bit 1 VB_LO_INT: VCCA low voltage interrupt status.
- Bit 0 PWRON_RISE_INT: PWRON pin rising edge interrupt status.

Note: 1: interrupt, write "1" to clear. 0: no interrupt

● INT_MSK_REG(REG[4D]): Interrupt Mask Register

| Address: 4DH | | | | Type: RW | | | | |
|--------------|---------------|---------------|--------------|-----------|-------------|----------|----------|---------------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | PWRON_FALL_IM | RTC_PERIOD_IM | RTC_ALARM_IM | HOTDIE_IM | PWRON_LP_IM | PWRON_IM | VB_LO_IM | PWRON_RISE_IM |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Description

- Bit 7 PWRON_FALL_IM: PWRON pin falling edge interrupt mask.
- Bit 6 RTC_PERIOD_IM: RTC period interrupt mask.
- Bit 5 RTC_ALARM_IM: RTC alarm interrupt mask.
- Bit 4 HOTDIE_IM: Hot-die interrupt mask.
- Bit 3 PWRON_LP_IM: PWRON long press interrupt mask.
- Bit 2 PWRON_IM: PWRON interrupt mask.
- Bit 1 VB_LO_IM: VCCA low voltage interrupt mask.
- Bit 0 PWRON_RISE_IM: PWRON pin rising edge interrupt mask.

Note: 1: mask the interrupt, 0: don't mask the interrupt

● IO_POL_REG(REG[50]): IO Polarity Register

| Address: 50H | | | | Type: RW | | | | |
|--------------|------|------|------|----------|------|---------|---------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | | | SLP_SD | | SLP_POL | INT_POL | |

| | | | | | | | | |
|---------|---|---|---|---|---|---|---|---|
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
|---------|---|---|---|---|---|---|---|---|

Description

| | |
|---------|---|
| Bit 7-4 | RESV: reserved |
| Bit 4-3 | SLP_SD: SLEEP pin function set: 00: Null, 01: PMU goes to SLEEP mode, 1x: turn down the PMU. |
| Bit 1 | SLP_POL: SLEEP pin polarity set: 1: active high, 0: active low |
| Bit 0 | INT_POL: INT pin polarity set: 1: active high, 0: active low |

● OUT_REG(REG[52]): Digital OUT Register

| | | | | | | | | |
|--------------|------|------|------|----------|------|------|------|------|
| Address: 52H | | | | Type: RW | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | | | | | OUT2 | OUT1 | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Description

| | |
|---------|---|
| Bit 7-2 | RESV: reserved |
| Bit 1 | OUT2: OUT2 pin output logic level: 1: high level; 0: low level |
| Bit 0 | OUT1: OUT1 pin output logic level: 1: high level; 0: low level |

● ON_SOURCE_REG(REG[AE]): ON Source Register

| | | | | | | | | |
|--------------|--------------|-------|------------|--------------------|----------------------|------|------|------|
| Address: AEH | | | | Type: RO | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | ON_P WRON | ON_EN | ON_ RTC | RESTART _RESETB | RESTART_P WRON_LP | RESV | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Description

| | |
|---------|--|
| Bit 7 | ON_PWRON: PWRON pressed to turn on the PMU. |
| Bit 6 | ON_EN: EN rising edge to turn on the PMU. |
| Bit 5 | ON_RTC: RTC alarm to turn on the PMU. |
| Bit 4 | RESTART_RESETB: pull down RESETB pin to restart the PMU. |
| Bit 3 | RESTART_PWRON_LP: long press PWRON key to restart the PMU. |
| Bit 2-0 | RESV: reserved. |

● OFF_SOURCE_REG(REG[AF]): OFF Source Register

| | | | | | | | | |
|--------------|--------|----------------|-------------|----------------|-----------------|----------------------|-----------------------|----------------|
| Address: AFH | | | | Type: RO | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | OFF_EN | OFF_S YS_OV | OFF_T SD | OFF_S YS_UV | OFF_DE V_OFF | OFF_P WRON _LP | OFF_U SB_OV _UV | OFF_S YS_LO |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Description

| | |
|-------|---|
| Bit 7 | OFF_EN: EN low level to turn off the PMU. |
| Bit 6 | OFF_VBV: VCCA over voltage to turn off the PMU. |
| Bit 5 | OFF_TSD: over temperature to turn off the PMU. |

- Bit 4 OFF_VB_UV: VCCA under voltage to turn off the PMU.
 Bit 3 OFF_DEV_OFF: write Reg4B<0>=1 to turn off the PMU.
 Bit 2 OFF_PWRON_LP: Long press PWRON key to turn off the PMU.
 Bit 1 OFF_SLEEP_SD: SLEEP active and Reg50<3:2>=1x to turn off the PMU.
 Bit 0 OFF_VB_LO: VCCA over voltage and Reg21<4>=0 to turn off the PMU.

5.2.4 Power Channel Control/Monitor Registers

● DCDC_EN_REG : DC-DC Converter Enable Register

| | | | | | | | | |
|--------------|---------------|---------------|---------------|---------------|-----------------------|----------|----------|----------|
| Address: 23H | | | | Type: RW | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | BUCK4_EN_MASK | BUCK3_EN_MASK | BUCK2_EN_MASK | BUCK1_EN_MASK | BUCK4_EN | BUCK3_EN | BUCK2_EN | BUCK1_EN |
| Default | 0 | 0 | 0 | 0 | Boot0:1111; Boot1:OTP | | | |

Description

- Bit 7-4 BUCK(n)_EN_MASK: BUCKn enable mask
 1, BUCK(n)_EN can be wrote
 0, BUCK(n)_EN can't be wrote
 Bit 3-0 BUCK(n)_EN: BUCKn enable
 1, Enable
 0, Disable
 The default value is set by boot.

● SLEEP_DCDC_EN_REG1: Sleep Mode DC-DC Converter Enable Register

| | | | | | | | | |
|--------------|------|------|------|----------|-----------------------|--------------|--------------|--------------|
| Address: 25H | | | | Type: RW | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | | | | BUCK4_EN_SLP | BUCK3_EN_SLP | BUCK2_EN_SLP | BUCK1_EN_SLP |
| Default | 0 | 0 | 0 | 0 | Boot0:1111; Boot1:OTP | | | |

Description

- Bit 7-4 Reserved
 Bit 3-0 BUCK(n)_EN_SLP: BUCKn enable at sleep mode
 1, Enable
 0, Disable
 The default value is set by boot.

● SLEEP_LDO_EN_REG : Sleep Mode LDO Enable Register

| | | | | | | | | |
|--------------|------|------|------|----------|------|----------------------|-------------|-------------|
| Address: 26H | | | | Type: RW | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | | | | | LDO3_EN_SLP | LDO2_EN_SLP | LDO1_EN_SLP |
| Default | 0 | 0 | 0 | 0 | 0 | Boot0:111; Boot1:OTP | | |

Description

- Bit 7-3 Reserved.
 Bit 2-0 LDO(n)_EN_SLP: LDO enable at sleep mode

1, Enable
0, Disable

● LDO_EN_REG : LDO Enable Register

| | | | | | | | | |
|--------------|------|--------------|--------------|--------------|------|----------------------|---------|---------|
| Address: 27H | | | | Type: RW | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | LDO3_EN_MASK | LDO2_EN_MASK | LDO1_EN_MASK | RESV | LDO3_EN | LDO2_EN | LDO1_EN |
| Default | 0 | 0 | 0 | 0 | 0 | Boot0:111; Boot1:OTP | | |

Description

Bit 7 Reserved.
 Bit 6-4 LDO(n)_EN_MASK: LDO enable mask
 1, LDO(n)_EN can be wrote
 0, LDO(n)_EN can't be wrote
 Bit 3 Reserved.
 Bit 2-0 LDO(n)_EN: LDO enable
 1, Enable
 0, Disable

● BUCK_LDO_SLP_LP_REG: BUCK And LDO Sleep Low Power Mode Register

| | | | | | | | | |
|--------------|-------------------------|------|------|----------|------|---------------|----------------|---------------|
| Address: 2AH | | | | Type: RW | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | BUCK12_PAR_ALWAYS_ON_EN | RESV | | | | BUCK12_PAR_EN | BUCK_SLP_LP_EN | LDO_SLP_LP_EN |
| Default | 0 | 0 | 0 | 0 | 0 | OTP | 0 | 0 |

Description

Bit 7 BUCK12_PAR_ALWAYS_ON_EN:
 1: BUCK1 and BUCK2 work together during light load when in parallel
 0: Only BUCK1 work during light load when in parallel
 Bit 6-3 RESV: reserved
 Bit 2 BUCK12_PAR_EN:
 1: enable BUCK1 and BUCK2 work in parallel, 0: disable
 Bit 1 BUCK_SLP_LP_EN:
 1: enable BUCK work in low power mode in sleep mode, 0:disable
 Bit 0 LDO_SLP_LP_EN:
 1: enable LDO work in low power mode in sleep mode, 0: disable

5.2.5 BUCK and LDO Configure Register

● BUCK1_CONFIG_REG: BUCK1 Configure Register

| | | | | | | | | |
|--------------|-------------|------|------------------|------------|------|-------------|------|------|
| Address: 2EH | | | | Type: RW | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | BUCK1_ILMAX | | BUCK1_DISCHRG_EN | BUCK1_RATE | | BUCK1_ILMIN | | |
| Default | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |

Description

Bit 7-6 BUCK1_ILMAX: BUCK1 maximum inductor's peak current limit

- 00: 2.5A, 01: 3A, 10: 3.5A, 11: 4A
- Bit 5 BUCK1_DISCHRG_EN: BUCK1 discharge resistor enable bit when shut down
0: disable discharge resistor when shut down
1: enable discharge resistor when shut down
- Bit 4-3 BUCK1_RATE: BUCK1 voltage change rate when DVS
00: 3mV/uS, 01: 6mV/uS, 10: 12.5mV/uS, 11: 25mV/uS
- Bit 2-0 BUCK1_ILMIN: BUCK1 minmum inductor's peak current
000: 150mA, 001: 200mA, 010: 250mA, 011: 300mA
100: 340mA, 101: 380mA, 110: 420mA, 111: 460mA

● **BUCK1_ON_VSEL_REG: BUCK1 Active Mode Register**

| | | | | | | | | |
|--------------|---------------|-------------|-------------------------|----------|------|------|------|------|
| Address: 2FH | | | | Type: RW | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | BUCK1_ON_FPWM | BUCK1_PHASE | BUCK1_ON_VSEL | | | | | |
| Default | 0 | 0 | Boot0:010111; Boot1:OTP | | | | | |

Description

- Bit 7 BUCK1_ON_FPWM:
1: force PWM mode in active mode
0: PWM/PFM auto change mode(default)
- Bit 6 BUCK1_PHASE:
0: normal, 1: inverted
- Bit 5-0 BUCK1_ON_VSEL: BUCK1 active mode voltage, 0.7125V~1.45V, step=12.5mV
000 000: 0.7125V
000 001: 0.725V
.....
111 011: 1.45V

111 100: 1.8V
111 101: 2.0V
111 110: 2.2V
111 111: 2.3V

● **BUCK1_SLP_VSEL_REG: BUCK1 Sleep Mode Register**

| | | | | | | | | |
|--------------|----------------|------|-------------------------|----------|------|------|------|------|
| Address: 30H | | | | Type: RW | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | BUCK1_SLP_FPWM | RESV | BUCK1_SLP_VSEL | | | | | |
| Default | 0 | 0 | Boot0:010111; Boot1:OTP | | | | | |

Description

- Bit 7 BUCK1_SLP_FPWM:
1: force PWM mode in sleep mode
0: PWM/PFM auto change mode(default)
- Bit 6 RESV: Reserved
- Bit 5-0 BUCK1_SLP_VSEL: BUCK1 sleep mode voltage , 0.7125V~1.45V, step=12.5mV
000 000: 0.7125V
000 001: 0.725V
.....
111 011: 1.45V

111 100: 1.8V
111 101: 2.0V
111 110: 2.2V

111 111: 2.3V

● BUCK2_CONFIG_REG: BUCK2 Configure Register

| | | | | | | | | |
|--------------|-------------|------|----------------------|------------|------|-------------|------|------|
| Address: 32H | | | | Type: RW | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | BUCK2_ILMAX | | BUCK2_DIS CHRG_EN | BUCK2_RATE | | BUCK2_ILMIN | | |
| Default | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |

Description

- Bit 7-6 BUCK2_ILMAX: BUCK2 maximum inductor's peak current limit
00: 2.5A, 01: 3A, 10: 3.5A, 11: 4A
- Bit 5 BUCK2_DISCHRG_EN: BUCK2 discharge resistor enable bit when shut down
0: disable discharge resistor when shut down
1: enable discharge resistor when shut down
- Bit 4-3 BUCK2_RATE: BUCK2 voltage change rate when DVS
00: 3mV/uS, 01: 6mV/uS, 10: 12.5mV/uS, 11: 25mV/uS
- Bit 2-0 BUCK2_ILMIN: BUCK2 minmum inductor's peak current
000: 150mA, 001: 200mA, 010: 250mA, 011: 300mA
100: 340mA, 101: 380mA, 110: 420mA, 111: 460mA

● BUCK2_ON_VSEL_REG: BUCK2 Active Mode Register

| | | | | | | | | |
|--------------|-------------------|---------------------|-------------------------|----------|------|------|------|------|
| Address: 33H | | | | Type: RW | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | BUCK2_O N_FPWM | BUCK2 _PHAS E | BUCK2_ON_VSEL | | | | | |
| Default | 0 | 0 | Boot0:010111; Boot1:OTP | | | | | |

Description

- Bit 7 BUCK2_ON_FPWM:
1: force PWM mode in active mode
0: PWM/PFM auto change mode(default)
- Bit 6 BUCK2_PHASE:
0: normal, 1: inverted
- Bit 5-0 BUCK2_ON_VSEL: BUCK2 active mode voltage, 0.7125V~1.45V, step=12.5mV
000 000: 0.7125V
000 001: 0.725V
.....
111 011: 1.45V

111 100: 1.8V
111 101: 2.0V
111 110: 2.2V
111 111: 2.3V

● BUCK2_SLP_VSEL_REG: BUCK2 Sleep Mode Register

| | | | | | | | | |
|--------------|--------------------|------|----------------|----------|------|------|------|------|
| Address: 34H | | | | Type: RW | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | BUCK2_S LP_FPWM | RESV | BUCK2_SLP_VSEL | | | | | |

| | | | |
|---------|---|---|-------------------------|
| Default | 0 | 0 | Boot0:010111; Boot1:OTP |
|---------|---|---|-------------------------|

Description

| | |
|---------|--|
| Bit 7 | BUCK2_SLP_FPWM: 1: force PWM mode in sleep mode 0: PWM/PFM auto change mode(default) |
| Bit 6 | RESV: Reserved |
| Bit 5-0 | BUCK2_SLP_VSEL: BUCK2 sleep mode voltage, 0.7125V~1.45V, step=12.5mV 000 000: 0.7125V 000 001: 0.725V 111 011: 1.45V 111 100: 1.8V 111 101: 2.0V 111 110: 2.2V 111 111: 2.3V |

● BUCK3_CONFIG_REG: BUCK3 Configure Register

| Address: 36H | | | | Type: RW | | | | |
|--------------|---------------|-------------|------------------|-------------|------|-------------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | BUCK3_ON_FPWM | BUCK3_PHASE | BUCK3_DISCHRG_EN | BUCK3_ILMAX | | BUCK3_ILMIN | | |
| Default | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |

Description

| | |
|---------|---|
| Bit 7 | BUCK3_ON_FPWM: 1: force PWM mode 0: PWM/PFM auto change mode(default) |
| Bit 6 | BUCK3_PHASE: 0: normal, 1: inverted |
| Bit 5 | BUCK3_DISCHRG_EN: BUCK3 discharge resistor enable bit when shut down 0: disable discharge resistor when shut down 1: enable discharge resistor when shut down |
| Bit 4-3 | BUCK3_ILMAX: BUCK3 maximum inductor's peak current limit 00: 1.5A, 01: 2A, 10: 2.5A, 11: 3A |
| Bit 2-0 | BUCK3_ILMIN: BUCK3 minimum inductor's peak current 000: 50mA, 001: 100mA, 010: 150mA, 011: 200mA 100: 250mA, 101: 300mA, 110: 350mA, 111: 400mA |

● BUCK4_CONFIG_REG: BUCK4 Configure Register

| Address: 37H | | | | Type: RW | | | | |
|--------------|------|-------------|------------------|-------------|------|-------------|------|------|
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | BUCK4_PHASE | BUCK4_DISCHRG_EN | BUCK4_ILMAX | | BUCK4_ILMIN | | |
| Default | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |

Description

| | |
|---------|---|
| Bit 7 | RESV: Reserved |
| Bit 6 | BUCK4_PHASE: 0: normal, 1: inverted |
| Bit 5 | BUCK4_DISCHRG_EN: BUCK4 discharge resistor enable bit when shut down 0: disable discharge resistor when shut down 1: enable discharge resistor when shut down |
| Bit 4-3 | BUCK4_ILMAX: BUCK4 maximum inductor's peak current limit |

00: 2A, 01: 2.5A, 10: 3A, 11: 3.5A

Bit 2-0 BUCK4_ILMIN: BUCK4 minmum inductor's peak current
 000: 50mA, 001: 100mA, 010: 150mA, 011: 200mA
 100: 250mA, 101: 300mA, 110: 350mA, 111: 400mA

● **BUCK4_ON_VSEL_REG: BUCK4 Active Mode Register**

| | | | | | | | | |
|--------------|---------------|------|------|------------------------|------|------|------|------|
| Address: 38H | | | | Type: RW | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | BUCK4_ON_FPWM | RESV | | BUCK4_ON_VSEL | | | | |
| Default | 0 | 0 | 0 | Boot0:11001; Boot1:OTP | | | | |

Description

Bit 7 BUCK4_ON_FPWM:
 1: force PWM mode in active mode
 0: PWM/PFM auto change mode(default)

Bit 6-5 RESV: Reserved

Bit 4-0 BUCK4_ON_VSEL: BUCK4 active mode voltage, 0.8V~3.5V, step=100mV
 00000: 0.8V
 00001: 0.9V

 11001: 3.3V
 11010: 3.4V
 11011: 3.5V
 111xx: 3.5V

● **BUCK4_SLP_VSEL: BUCK4 Sleep Mode Register**

| | | | | | | | | |
|--------------|----------------|------|------|------------------------|------|------|------|------|
| Address: 39H | | | | Type: RW | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | BUCK4_SLP_FPWM | RESV | | BUCK4_SLP_VSEL | | | | |
| Default | 0 | 0 | 0 | Boot0:11001; Boot1:OTP | | | | |

Description

Bit 7 BUCK4_SLP_FPWM:
 1: force PWM mode in sleep mode
 0: PWM/PFM auto change mode(default)

Bit 6-5 RESV: Reserved

Bit 4-0 BUCK4_SLP_VSEL:BUCK4 sleep mode voltage, 0.8V~3.5V, step=100mV
 00000: 0.8V
 00001: 0.9V

 11001: 3.3V
 11010: 3.4V
 11011: 3.5V
 111xx: 3.5V

● **LDO1_ON_VSEL_REG: LDO1 Active Voltage Selection Register**

| | | | | | | | | |
|--------------|------|-----------|-----------------|------------------------|------|------|------|------|
| Address: 3BH | | | | Type: RW | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | LDO1_IMAX | LDO1_DISCHRG_EN | LDO1_ON_VSEL | | | | |
| Default | 0 | 0 | 1 | Boot0:00010; Boot1:OTP | | | | |

Description

| | |
|---------|---|
| Bit 7 | RESV: Reserved |
| Bit 6 | LDO1_IMAX: LDO1 current limit 0: nomal, 1: 130%*nomal |
| Bit 5 | LDO1_DISCHRG_EN: LDO1 discharge resistor enable bit when shut down 0: disable discharge resistor when shut down 1: enable discharge resistor when shut down |
| Bit 4-0 | LDO1_ON_VSEL: LDO1 active mode voltage, 0.8V~3.4V, step=0.1V 00000: 0.8V 00001: 0.9V 11001: 3.3V 11010: 3.4V |

● **LDO1_SLP_VSEL_REG: LDO1 Sleep Voltage Selection Register**

| | | | | | | | | |
|--------------|------|------|------|------------------------|------|------|------|------|
| Address: 3CH | | | | Type: RW | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | | | LDO1_SLP_VSEL | | | | |
| Default | 0 | 0 | 0 | Boot0:00010; Boot1:OTP | | | | |

Description

| | |
|---------|--|
| Bit 7-5 | RESV: Reserved |
| Bit 4-0 | LDO1_SLP_VSEL: LDO1 sleep mode voltage, 0.8V~3.4V, step=0.1V 00000: 0.8V 00001: 0.9V 11001: 3.3V 11010: 3.4V |

● **LDO2_ON_VSEL_REG: LDO2 Active Voltage Selection Register**

| | | | | | | | | |
|--------------|------|-----------|-----------------|------------------------|------|------|------|------|
| Address: 3DH | | | | Type: RW | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | LDO2_IMAX | LDO2_DISCHRG_EN | LDO2_ON_VSEL | | | | |
| Default | 0 | 0 | 1 | Boot0:01010; Boot1:OTP | | | | |

Description

| | |
|---------|---|
| Bit 7 | RESV: Reserved |
| Bit 6 | LDO2_IMAX: LDO2 current limit 0: nomal, 1: 130%*nomal |
| Bit 5 | LDO2_DISCHRG_EN: LDO2 discharge resistor enable bit when shut down 0: disable discharge resistor when shut down 1: enable discharge resistor when shut down |
| Bit 4-0 | LDO2_ON_VSEL: LDO2 active mode voltage, 0.8V~3.4V, step=0.1V 00000: 0.8V 00001: 0.9V 11001: 3.3V 11010: 3.4V |

● **LDO2_SLP_VSEL_REG: LDO2 Sleep Voltage Selection Register**

| | | | | | | | | |
|--------------|------|------|------|----------|------|------|------|------|
| Address: 3EH | | | | Type: RW | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |

| | | | | |
|---------|------|---|---|------------------------|
| SYMBOL | RESV | | | LDO2_SLP_VSEL |
| Default | 0 | 0 | 0 | Boot0:01010; Boot1:OTP |

Description

Bit 7-5 RESV: Reserved
 Bit 4-0 LDO2_SLP_VSEL: LDO2 sleep mode voltage, 0.8V~3.4V, step=0.1V
 00000: 0.8V
 00001: 0.9V

 11001: 3.3V
 11010: 3.4V

● LDO3_ON_VSEL_REG: LDO3 Active Voltage Selection Register

| | | | | | | | | |
|--------------|------|-----------|-----------------|------------------------|------|------|------|------|
| Address: 3FH | | | | Type: RW | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | LDO3_IMAX | LDO3_DISCHRG_EN | LDO3_ON_VSEL | | | | |
| Default | 0 | 0 | 1 | Boot0:00010; Boot1:OTP | | | | |

Description

Bit 7 RESV: Reserved
 Bit 6 LDO3_IMAX: LDO3 current limit
 0: nomal, 1: 130%*nomal
 Bit 5 LDO3_DISCHRG_EN: LDO3 discharge resistor enable bit when shut down
 0: disable discharge resistor when shut down
 1: enable discharge resistor when shut down
 Bit 4-0 LDO3_ON_VSEL: LDO3 active mode voltage, 0.8V~3.4V, step=0.1V
 00000: 0.8V
 00001: 0.9V

 11001: 3.3V
 11010: 3.4V

● LDO3_SLP_VSEL_REG:LDO3 Sleep Voltage Selection Register

| | | | | | | | | |
|--------------|------|------|------|------------------------|------|------|------|------|
| Address: 40H | | | | Type: RW | | | | |
| Bit | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| SYMBOL | RESV | | | LDO3_SLP_VSEL | | | | |
| Default | 0 | 0 | 0 | Boot0:00010; Boot1:OTP | | | | |

Description

Bit 7-5 RESV: Reserved
 Bit 4-0 LDO3_SLP_VSEL: LDO3 sleep mode voltage, 0.8V~3.4V, step=0.1V
 00000: 0.8V
 00001: 0.9V

 11001: 3.3V
 11010: 3.4V

Chapter 6 Thermal Management

6.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature of RK805 has to be below 125°C.

Depending on the thermal mechanical design (Smartphone, Tablet, Personal Navigation Device, etc), the system thermal management software and worst case thermal applications, the junction temperature might be exposed to higher values than those specified above.

Therefore, it is recommended to perform thermal simulations at device level (Smartphone, Tablet, Personal Navigation Device, etc) with the measured power of the worst case UC of the device.

6.2 Package Thermal Characteristics

Table 6-1 provides the thermal resistance characteristics for the package used on this device.

Table 6-1 Thermal Resistance Characteristics

| PACKAGE (QFN4X4-32) | POWER(W) | θ_{JA}(°C/W) | θ_{JB}(°C/W) | θ_{JC}(°C/W) |
|--------------------------------|-----------------|---------------------------------------|---------------------------------------|---------------------------------------|
| RK805 | 2 | 45 | 21 | 2 |

Note: The testing PCB is based on 4 layers, 114mm x 76 mm, 1.6mm thickness, Ambient temperature is 85°C.